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-	5005	((model$4 or simulat$4 or emulat$4) and (FET or (field adj effect adj transistor?)) and (source and gate and drain)) and state	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 13:49
-	277	((model$4 or simulat$4 or emulat$4) and (FET or (field adj effect adj transistor?)) and (source and gate and drain)) and (state adj machine)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 13:49
-	236	((model$4 or simulat$4 or emulat$4) same (FET or (field adj effect adj transistor?)) same (source and gate and drain)) and state	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 13:50
-	4873	(((model$4 or simulat$4 or emulat$4) and (FET or (field adj effect adj transistor?)) and (source and gate and drain)) and state) and (body voltage)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 13:50
-	52	(((model$4 or simulat$4 or emulat$4) and (FET or (field adj effect adj transistor?)) and (source and gate and drain)) and state) and (body adj voltage)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 13:51
-	8	((((model$4 or simulat$4 or emulat$4) and (FET or (field adj effect adj transistor?)) and (source and gate and drain)) and state) and (body adj voltage)) and (partial$2 adj deplet$2)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 13:52
-	9	((((model$4 or simulat$4 or emulat$4) and (FET or (field adj effect adj transistor?)) and (source and gate and drain)) and state) and (body adj voltage)) and (partially same depleted)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:05
-	4	SHEPARD-KENNETH-B	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:05
-	1	SHEPARD-KENNETH-W	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:06
-	46	SHEPARD-KENNETH-L	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:10
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-	2	6023577.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:13
-	2	6023577.uref.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:13
-	8	((((model$4 or simulat$4 or emulat$4) and (FET or (field adj effect adj transistor?)) and (source and gate and drain)) and state) and (body adj voltage)) and (partial$4 adj deplet$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:43
-	0	SHEPARD-KENNETH-L and soi	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:10
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-	41	(soi or (silicon near3 insulator?)) and (fet or (field near3 effect?)) and state? and (body near2 voltage?)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:21
-	60	(soi or (silicon near3 insulator?)) and (fet or (field near3 effect?)) and state$1 and (body near2 voltage?)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:21
-	275	(soi or (silicon near3 insulator$1)) and (fet or (field near3 effect$1)) and state$1 and (body near2 voltage$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:21
-	257	(soi or (silicon near3 insulator$1)) and (fet or (field near3 effect$1)) and state$1 and (body near2 voltage$1) and (source$1 and gate$1 and drain$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:22
-	116	((soi or (silicon near3 insulator$1)) and (fet or (field near3 effect$1)) and state$1 and (body near2 voltage$1) and (source$1 and gate$1 and drain$1)) and (model$4 or simulat$4 or emulat$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:42
-	114	(((soi or (silicon near3 insulator$1)) and (fet or (field near3 effect$1)) and state$1 and (body near2 voltage$1) and (source$1 and gate$1 and drain$1)) and (model$4 or simulat$4 or emulat$4)) and tim$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:43
-	49	(((soi or (silicon near3 insulator$1)) and (fet or (field near3 effect$1)) and state$1 and (body near2 voltage$1) and (source$1 and gate$1 and drain$1)) and (model$4 or simulat$4 or emulat$4)) and timing	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:42
-	34	(((soi or (silicon near3 insulator$1)) and (fet or (field near3 effect$1)) and state$1 and (body near2 voltage$1) and (source$1 and gate$1 and drain$1)) and (model$4 or simulat$4 or emulat$4)) and transition$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:43

| | | 4 | (((soi or (silicon near3 insulator$1)) and (fet or (field near3 effect$1)) and state$1 and (body near2 voltage$1) and (source$1 and gate$1 and drain$1)) and (model$4 or simulat$4 or emulat$4)) and (state adj transition$1) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/07/25 15:43 |

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1 **Body-voltage estimation in digital PD-SOI circuits and its application to static timing analysis**
Shepard, K.L.; Dae-Jin Kim;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 20 Issue: 7 , July 2001
Page(s): 888 -901

[Abstract]   [PDF Full-Text (308 KB)] **IEEE JNL**

2 **Body-voltage estimation in digital PD-SOI circuits and its application to static timing analysis**
Shepard, K.L.; Dae-Jin Kim;
Computer-Aided Design, 1999. Digest of Technical Papers. 1999 IEEE/ACM International Conference on , 7-11 Nov. 1999
Page(s): 531 -538

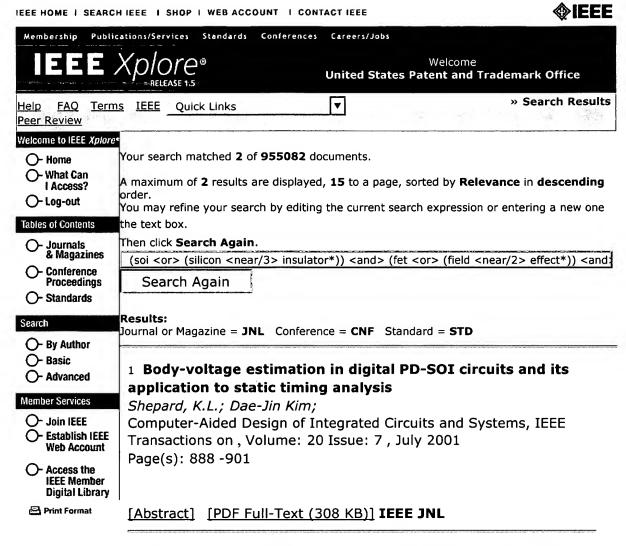[Abstract]   [PDF Full-Text (772 KB)] **IEEE CNF**

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Mayer, D.C.; Cole, R.C.; Pollack, G.P.;
Electron Devices Meeting, 1991. Technical Digest., International ,
8-11 Dec. 1991
Page(s): 329 -332

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2 **Parasitic bipolar transistor induced latch and degradation in SOI MOSFET's**
Her, T.-D.; Liu, P.S.; Quon, D.S.; Li, G.P.; Kjar, R.; White, J.;
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Oct. 1991
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[Abstract]   [PDF Full-Text (120 KB)] **IEEE CNF**

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3 **Device performance analysis using Monte-Carlo simulator for SOI MOS transistors on solid-phase-recrystallized silicon films**
Kambayashi, S.; Mizushima, I.; Kemmochi, M.; Kawaguchi, H.; Shima, S.; Kuwano, H.; Onga, S.; Matsunaga, J.;
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on , 4-7 June 1990
Page(s): 109 -110

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4 **Thermal time constants in SOI-MOSFETs**
Berger, M.; Burbach, G.;
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Oct. 1991
Page(s): 24 -25

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5 **OFF-State leakage current mechanisms in bulkSi and SOI MOSFETs and their impact on CMOS ULSIs standby current**
Adan, A.O.; Higashi, K.;
Electron Devices, IEEE Transactions on , Volume: 48 Issue: 9 , Sept.
2001
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[Abstract]   [PDF Full-Text (220 KB)] **IEEE JNL**

6 **A simple model to predict the holding voltage for SOI MOSFETs operating in the latch state**
*McDaid, L.J.; Hall, S.; Marsland, J.S.; Eccleston, W.; Alderman, J.C.;
Cook, K.R.; Bunyan, R.J.; Uren, M.J.;*
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7 **Monte-Carlo modelling of a MISFET/SOI struck by an energetic heavy ion**
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Radiation and its Effects on Devices and Systems, 1991. RADECS
91., First European Conference on , 9-12 Sept. 1991
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8 **Conduction mechanisms in thin-film accumulation-mode SOI p-channel MOSFETs**
Colinge, J.-P.;
Electron Devices, IEEE Transactions on , Volume: 37 Issue: 3 , March
1990
Page(s): 718 -723

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9 **An analytic model for very thin SOI transistors**
McKitterick, J.B.; Caviglia, A.L.;
SOS/SOI Technology Workshop, 1988. Proceedings., 1988 IEEE , 3-5
Oct. 1988
Page(s): 41

[Abstract] [PDF Full-Text (56 KB)] **IEEE CNF**

10 **Two-dimensional numerical simulation of short channel SOI transistors**
Armstrong, G.A.; Thomas, N.J.; Davis, J.R.;
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Oct. 1988
Page(s): 48

[Abstract] [PDF Full-Text (52 KB)] **IEEE CNF**

11 **Surface potential at threshold, transconductance, and carrier generation in thin SOI MOSFETs**
Ioannou, D.E.; Mazhari, B.; Zhong, X.; Cristoloveanu, S.; Caviglia, A.L.;
SOS/SOI Technology Conference, 1990., 1990 IEEE , 2-4 Oct. 1990
Page(s): 95 -96

[Abstract] [PDF Full-Text (84 KB)] **IEEE CNF**

12 **Investigation of series resistances, interface coupling and irradiation effects on the transconductance of fully-depleted SOI-MOSFETs**
Ouisse, T.; Cristoloveanu, S.; Borel, G.;
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Oct. 1991
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[Abstract] [PDF Full-Text (116 KB)] **IEEE CNF**

13 **Fabrication & characterization of Schottky junction transistors**
Wu, Z.; Spann, J.; Jaconelli, P.C.; Jinman Yang; Thornton, T.J.;
SOI Conference, 2001 IEEE International , 1-4 Oct. 2001
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[Abstract] [PDF Full-Text (144 KB)] **IEEE CNF**

14 **Modeling and design of a low-voltage SOI suspended-gate MOSFET (SG-MOSFET) with a metal-over-gate architecture**
Ionescu, A.M.; Pott, V.; Fritschi, R.; Banerjee, K.; Declercq, M.J.;

Renaud, P.; Hibert, C.; Fluckiger, P.; Racine, G.A.;
Quality Electronic Design, 2002. Proceedings. International
Symposium on , 18-21 March 2002
Page(s): 496 -501

[Abstract]   [PDF Full-Text (1289 KB)] **IEEE CNF**

15 **Lateral insulated gate bipolar transistor (LIGBT) structure based on partial isolation SOI technology**
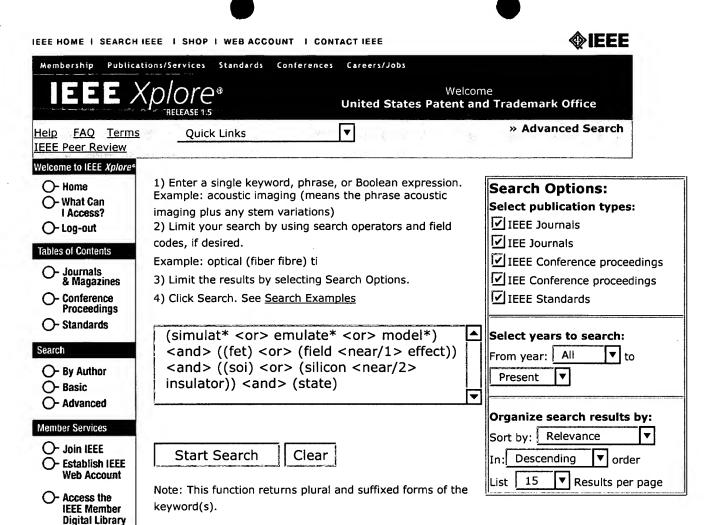*Udrea, F.; Milne, W.; Popescu, A.;*
Electronics Letters , Volume: 33 Issue: 10 , 8 May 1997
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*Kerns, S.E.; Shafer, B.D.; Rockett, L.R., Jr.; Pridmore, J.S.; Berndt,
D.F.; van Vonno, N.; Barber, F.E.;*
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[Abstract]   [PDF Full-Text (3652 KB)] **IEEE JNL**

2 **SOI transistor measurement techniques using body
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Worley, E.R.; Williams, R.;
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[Abstract]   [PDF Full-Text (468 KB)] **IEEE JNL**

3 **Ionization radiation induced degradation of MOSFET channel
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[Abstract]   [PDF Full-Text (572 KB)] **IEEE JNL**

4 **Elimination of kink effect in fully depleted complementary buried-channel SOL MOSFET (FD CBCMOS) based on silicon direct bonding technology**
Qin-Yi Tong; Xiao-Li Xu; Hui-Zhen Zhang;
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[Abstract]   [PDF Full-Text (236 KB)] **IEEE JNL**

5 **Device modelling and design techniques for analogue SOS circuits**
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12 **Accumulation mode transistors for silicon-on-insulator circuits**
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14 **Interface characterization in fully depleted SOI MOSFETs by dynamic transconductance**
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[Abstract]   [PDF Full-Text (100 KB)] **IEEE CNF**

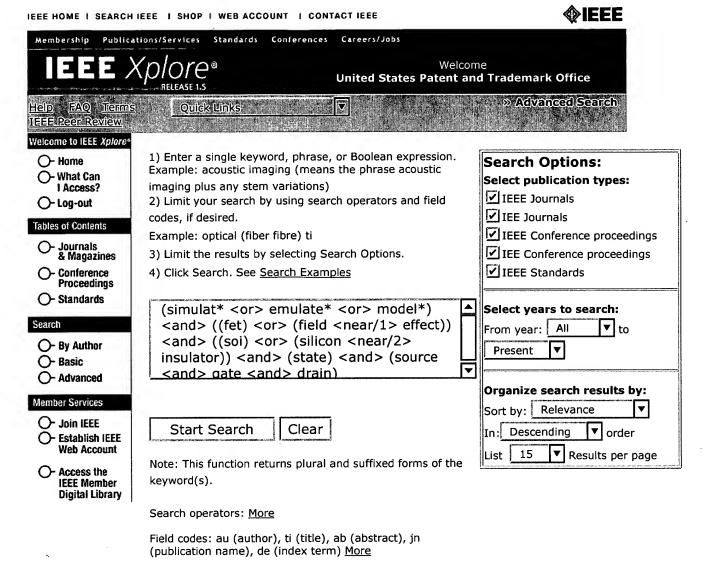15 **Noise overshoot at drain current kink in SOI MOSFET**
Chen, J.; Fang, P.; Ko, P.K.; Hu, C.; Solomon, R.; Chan, T.-Y.;
Sodini, C.G.;
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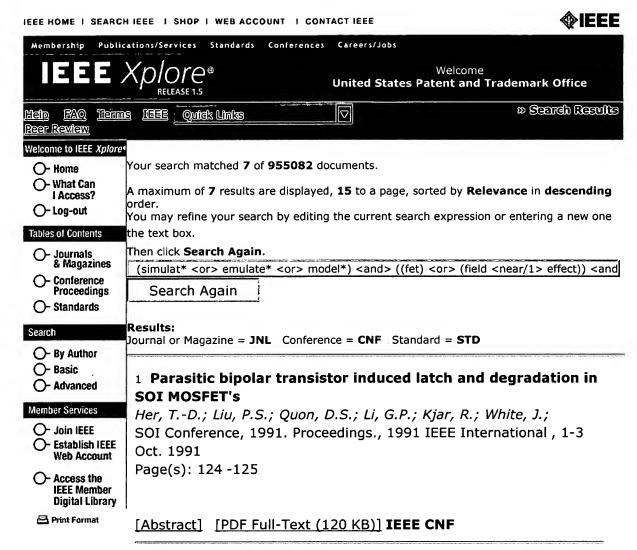[Abstract]   [PDF Full-Text (132 KB)] **IEEE CNF**

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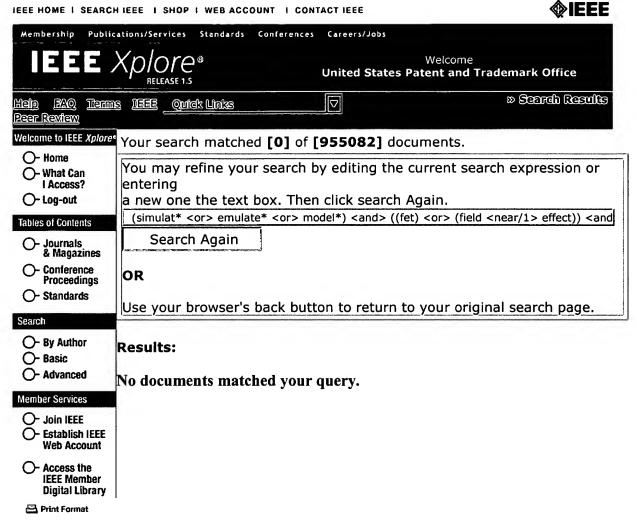In: | Descending ▼ | order
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Her, T.-D.; Liu, P.S.; Quon, D.S.; Li, G.P.; Kjar, R.; White, J.;
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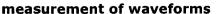4 **CAD issues for CMOS VLSI design in SOI**
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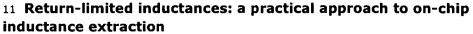*Shepard, K.L.; Dae-Jin Kim;*
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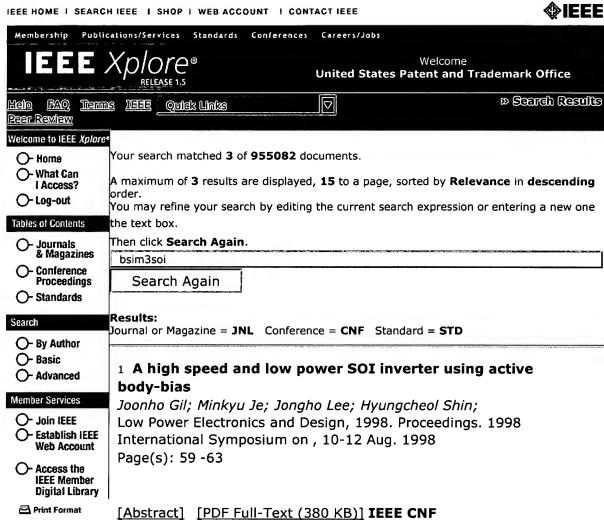
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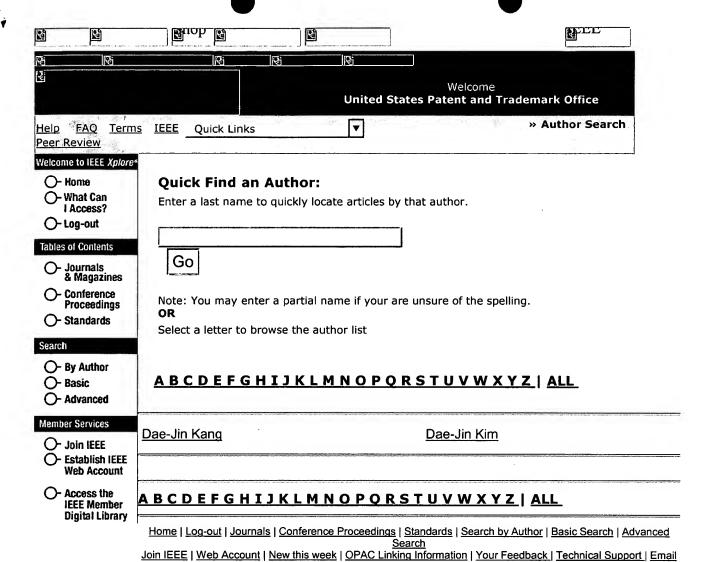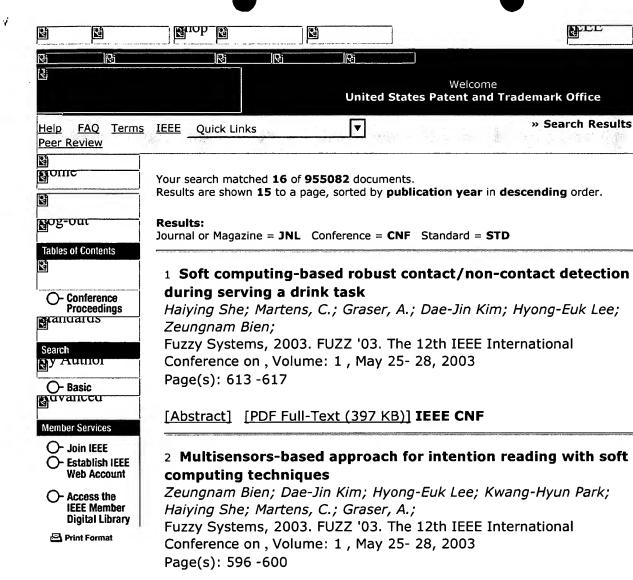
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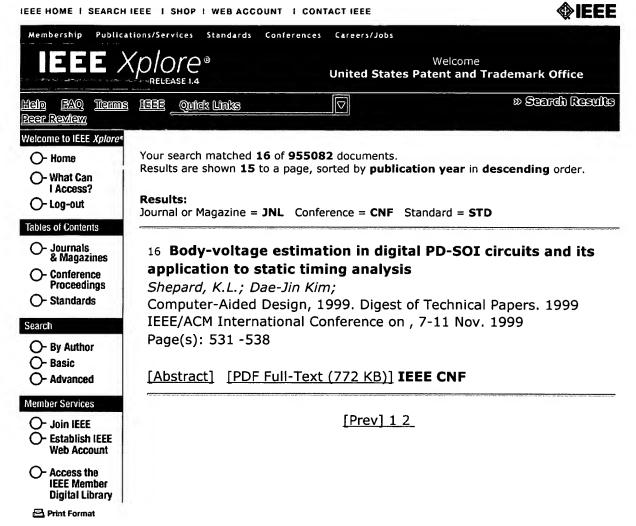Aug. 2000
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Ken Shepard received the B. S. E. degree from Princeton University, Princeton, NJ, in 1987 where he was valedictorian of his graduating class and received the Phi Beta Kappa prize for the highest academic standing. He went on to receive the M. S. and Ph. D. degrees in electrical engineering with a minor in physics from Stanford University, Stanford, CA, in 1988 and 1992, respectively, on a fellowship from the Fannie and John Hertz Foundation. His Ph. D. research, also funded by a special "Creativity in Engineering" grant from the National Science Foundation, focussed on the physics of nanoscale devices. He was awarded the Hertz Foundation doctoral thesis prize in 1992, given each year to the best Ph. D. thesis from among Hertz Fellows.

In 1992, he became a Research Staff Member in the VLSI Design Department at the IBM T. J. Watson Research Center, Yorktown Heights, NY and was promoted to Manager in 1996. At IBM, he was responsible for the design methodology for IBM's first high-performance microprocessors for the S/390 mainframe (Alliance project). This design methodology became the basis for subsequent microprocessor designs at IBM. He received IBM Research Division Awards in 1995 and 1997 for his contributions to the Alliance project team.

In 1997, he joined Columbia University, where he is now Associate Professor. At the same time, he co-founded CadMOS Design Technology, an EDA start-up which pioneered PacifIC and CeltIC, the first tools for large-scale signal integrity analysis of digital integrated circuits. The success of these tools led Cadence to acquire CadMOS in 2001.

Current research interests include design tools for advanced CMOS technology, including the CAD work in SOI circuits and extraction approaches for inductance that are being commercialized by

Cadence. Professor Shepard and his students are also working on on-chip test and measurement circuitry including on-chip sampling oscilloscopes, low-power design techniques for digital signal processing, circuits for low-power intrachip communications, and CMOS gene chips. He received the National Science Foundation CAREER Award in 1998, the Distinguished Faculty Teaching Award from the Columbia Engineering School in 1999, a Best Paper Award at the 2001 International Conference on Computer Design, best paper runner-up at the 2003 International Symposium on Asynchronous Circuits, and a winning entry in the 2003 ISLPED Low-Power Design Contest.

Professor Shepard is program chair for the 2002 International Conference on Computer Design (ICCD) and general chair of the 2003 ICCD. He was program chair of ISQED 2002 and conference co-chair of ISQED 2003 and has served on the program committees of DAC, ICCD, ICCAD, GLS-VLSI, ISQED, and Tau. He was Associate Editor of IEEE Transactions on VLSI from 1998-2001.

Research Activities

Please see my group website.

Prospective graduate students interested in research or teaching assistantships in my group may contact me in addition to visiting the graduate admissions web site.

A list of my publications can be found here.

Teaching

- EE E3106. Solid State Materials and Devices Fall, 1997
- EE E3201. Circuit Analysis Fall, 1997
- EE E4321. VLSI Circuits Fall, 1999 Fall, 2002
- EE E4332. VLSI Design Lab Spring, 1999 Spring, 2000
- EE E4340. Computer Hardware Design Spring, 1999
- EE E6930. Advanced Digital Integrated Circuits Spring, 2001